TSMC-03-281

March 9, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 10/758,315 01/15/04

Shin-Yeu Tsai et al.

SOLUTION FOR COPPER HILLOCK INDUCED BY THERMAL STRAIN WITH BUFFER ZONE FOR STRAIN RELAXATION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 16, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date SBA 3/16/04

U.S. Patent 5,654,232 to Gardner, "Wetting Layer Sidewalls to Promote Copper Reflow into Grooves," teaches a copper damascene process.

U.S. Patent 6,355,571 to Huang et al., "Method and Apparatus for Reducing Copper Oxidation and Contamination in a Semiconductor Device," discloses the use of NH3 or H2 to reduce CuO to copper and an in-situ deposition of a capping layer.

The following two U.S. Patents teach NH3 and N2 plasma to reduce CuO to Cu and an in-situ deposition of a capping layer:

1) U.S. Patent 6,506,677 to Avanzino et al., "Method of Forming Capped Copper Interconnects with Reduced Hillock Formation and Improved Electromigration Resistance."
2) U.S. Patent 6,429,128 to Besser et al., "Method of Forming Nitride Capped Cu Lines with Reduced Electromigration Along the Cu/Nitride Iinterface."

U.S. Patent 6,482,755 to Ngo et al., "HDP Deposition Hillock Suppression Method in Integrated Circuits," discloses treatment in NH3, NH2, or H2 plasma at a reduced temperature to reduce CuO to Cu, then in-situ deposition of HDP silicon nitride.

U.S. Patent 6,515,373 to Barth, "Cu-Pad/Bonded/Cu-Wire with Self-Passivating Cu-Alloys," describes annealing before and/or after CMP to reduce hillocks.

U.S. Patent 6,500,754 to Erb et al., "Anneal Hillock Suppression Method in Integrated Circuit Interconnects," discloses annealing prior to CMP wherein the annealing stimulates grain growth to prevent hillock formation.

Co-pending U.S. Patent Application TSMC-00-863, Serial No. 09/998,787, filed 10/31/01 to the same assignee, "A Solution to the Problem Copper Hillocks," discloses a method of reducing copper hillocks.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-03-281	10/758,315
Applicant: Shin-Yeu Tsai et al.	
Filing Date: 01/15/04	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5654232	8/5/97	Gardner	438	661	3/15/96
	6355571	3/12/02	Huang et al.	438	706	7/30/99
	6506677	1/14/03	Avanzino et al.	438	687	5/2/01
	6429128	8/6/02	Besser et al.	438	687	7/12/01
	6482755	11/19/02	Ngo et al.	438	792	6/12/01
	6515373	2/4/03	Barth	257	781	12/28/00
	6500754	12/31/02	Erb et al.	438	626	10/31/01

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Co-pending U.S. Patent Application TSMC-00-863, Serial No. 09/998,787, filed 10/31/01, to the same assignee, "A Solution to the Problem of Copper Hillocks".

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.